

1/6. FIG. 1

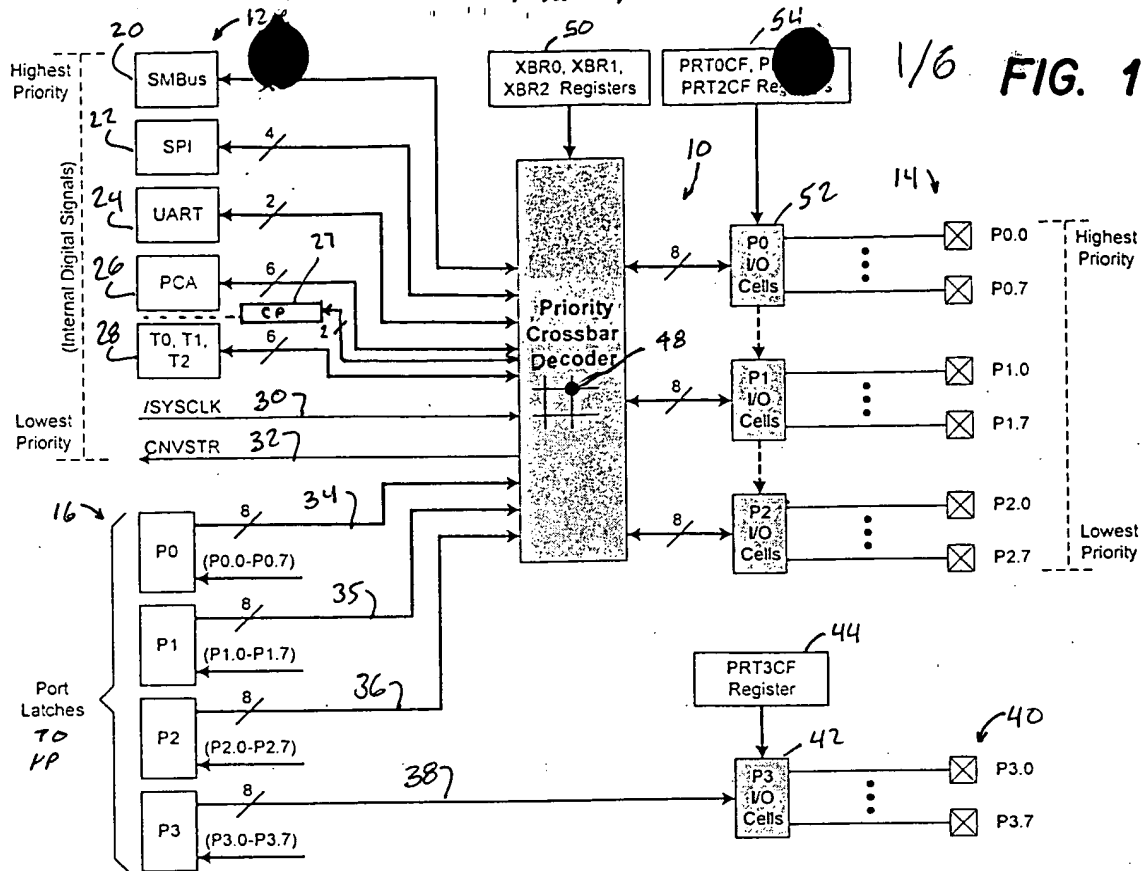
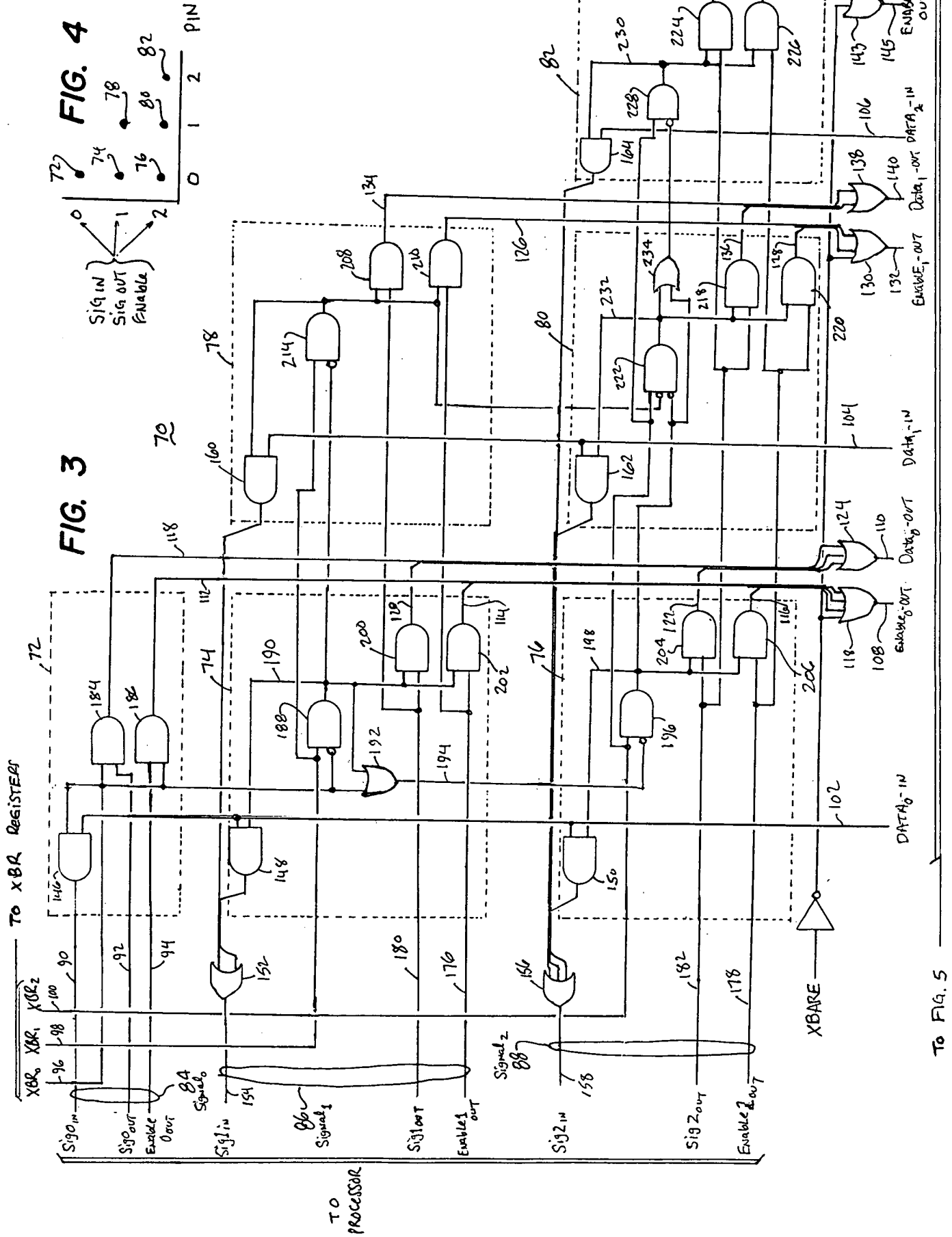
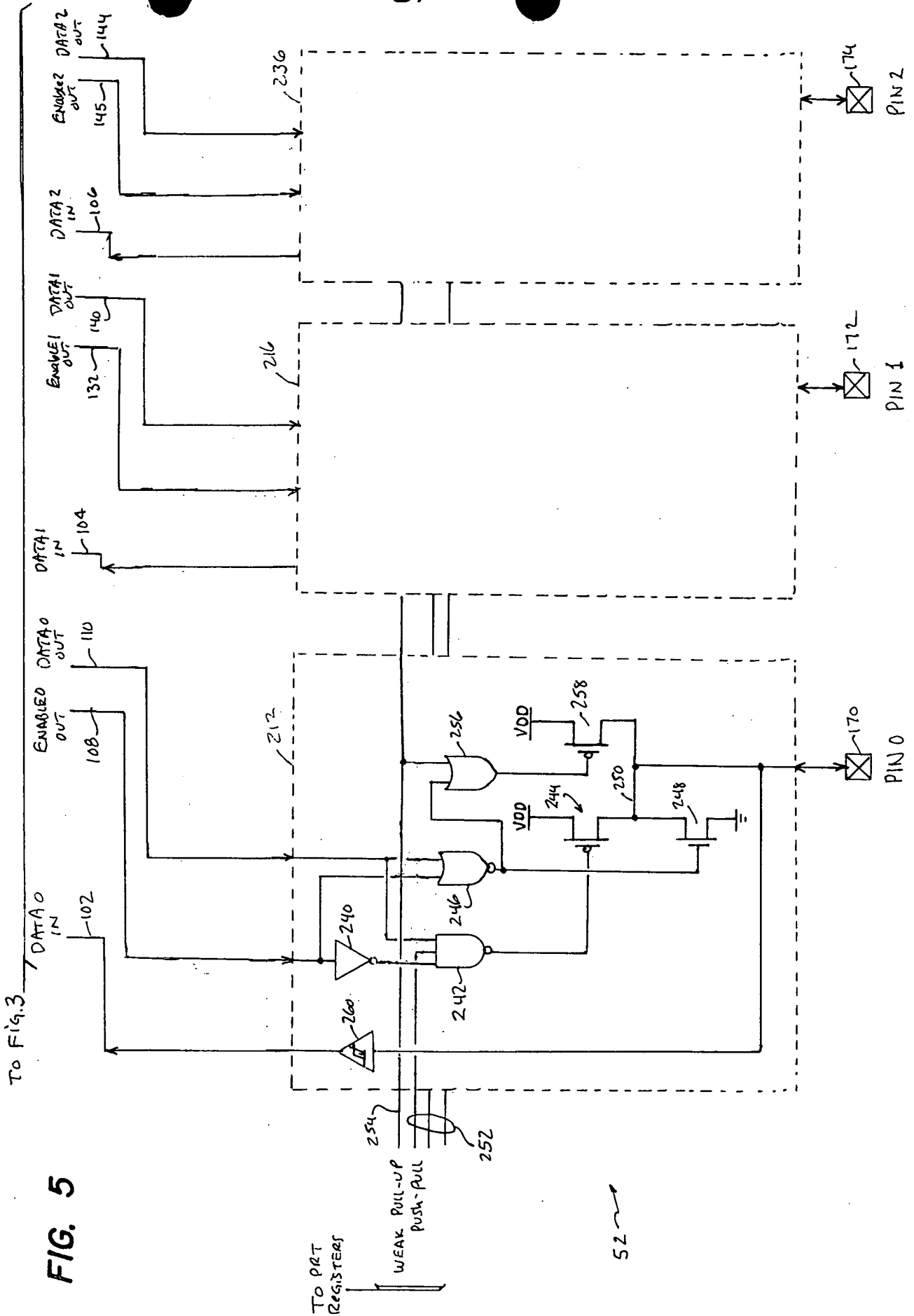


FIG. 2

		P0								P1								P2							
PIN I/O		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
20	SDA	●	✓	61																					
	SCL	●	✓	58																					
22	SCK	●		●																					
	MISO		●		●																				
	MOSI			●		●																			
	NSS				●		●																		
24	TX	●		●		●		●																	
	RX		●		●		●		●	✓	48														
26	CEX0	●		●		●		●		✓	56														
	CEX1		●		●		●		●		●														
	CEX2			●		●		●		●		●													
	CEX3				●		●		●		●		●												
	CEX4					●		●		●		●		●											
	ECI	●	●	●		●	●	●	●	●	●	●	●	●	●										
27	CP0	●	●	●	●		●	●	●	●	●	●	●	●	●	●									
	CP1	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●								
28	T0	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●							
	/INT0	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
	T1	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●					
	/INT1	●	●	●	●		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●				
	T2	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●			
	T2EX			●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
30	/SYSCLK	●	●	●	●		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
32	CNVSTR	●		●		●		●		●		●		●		●		●		●		●		●	





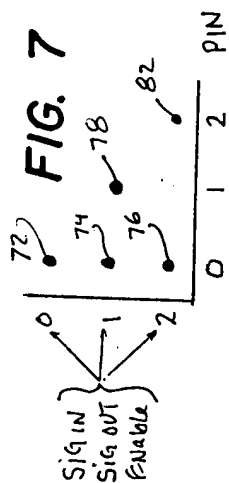
001E50"80E4B550

To XBR Register

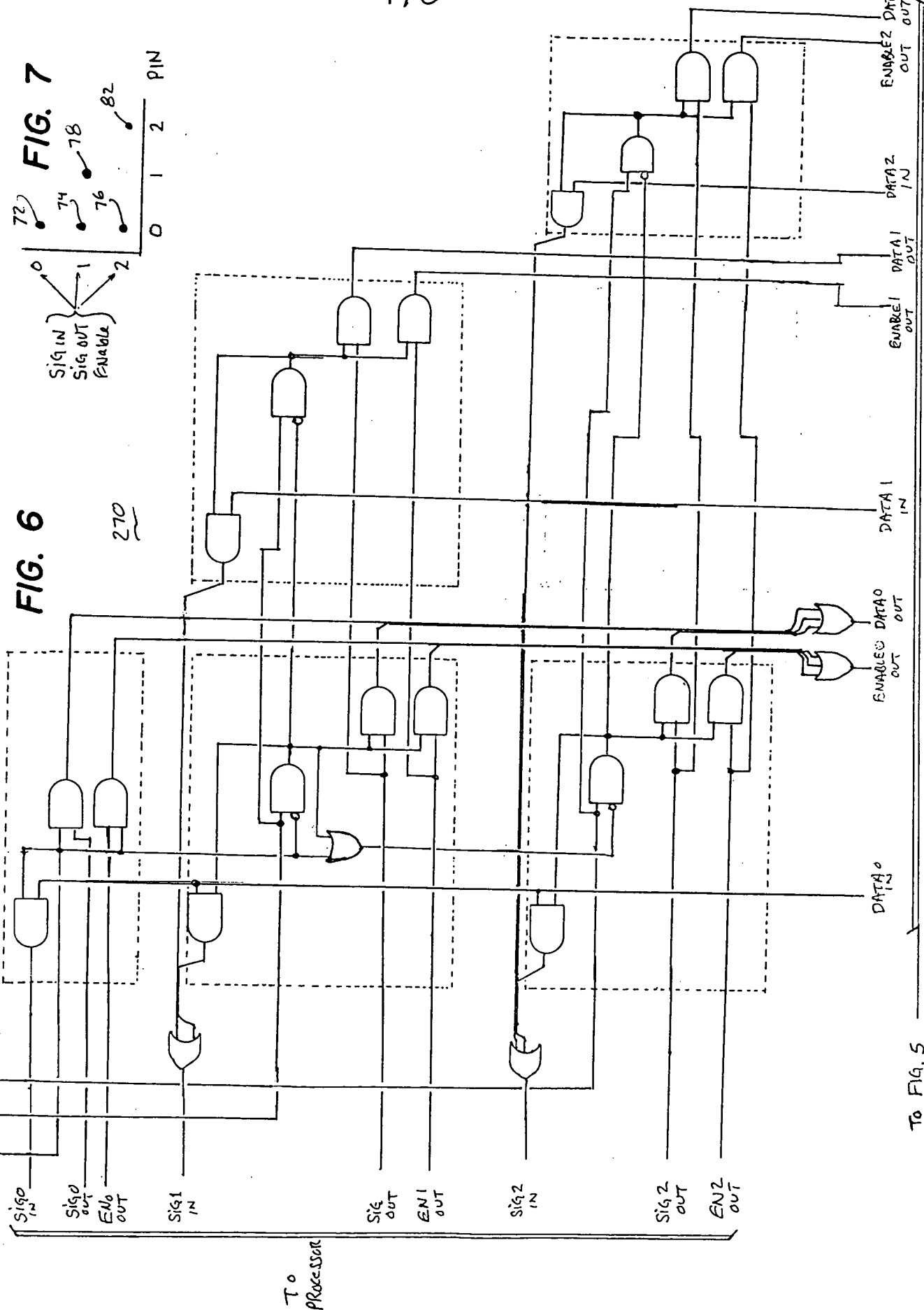
XBR₀ XBR₁ XBR₂

FIG. 6

FIG. 7



270



To FIG. 5



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FIG. 9

